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## (54) Method of manufacturing FET devices with maskless shallow trench isolation (STI)

(57) FET devices (10) are manufactured using STI on a semiconductor substrate (11) coated with a pad (14) from which are formed raised active silicon device areas and dummy active silicon mesas (12) capped with pad structures on the doped silicon substrate and pad structure. A conformal blanket silicon oxide (22) layer is deposited on the device (10) with conformal projections above the mesas (12). Then a polysilicon film (24) on the blanket silicon oxide layer (22) is deposited with conformal projections above the mesas (12). The polysilicon film projections are removed in a CMP polishing step which continues until the silicon oxide layer (22) is exposed over the pad structures (14). Selective RIE partial etching of the conformal silicon oxide layer (22) over the mesas (12) is next, followed in turn by CMP planarization of the conformal blanket silicon oxide layer (22) which converts the silicon oxide layer into a planar silicon oxide layer, using the pad silicon nitride (14) as an etch stop.

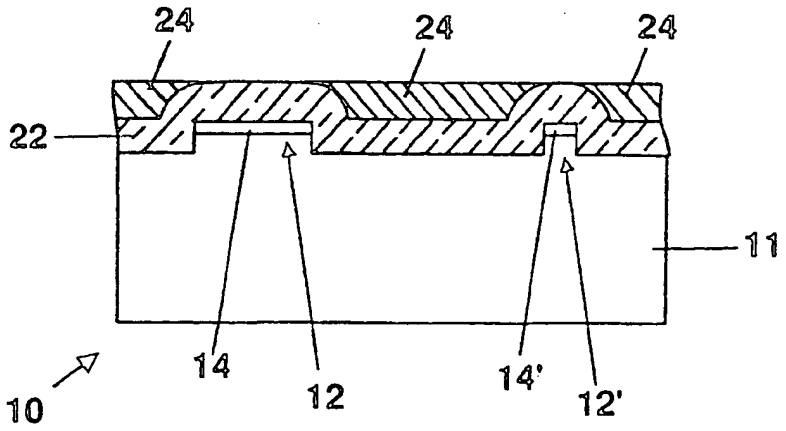


FIG. 1D

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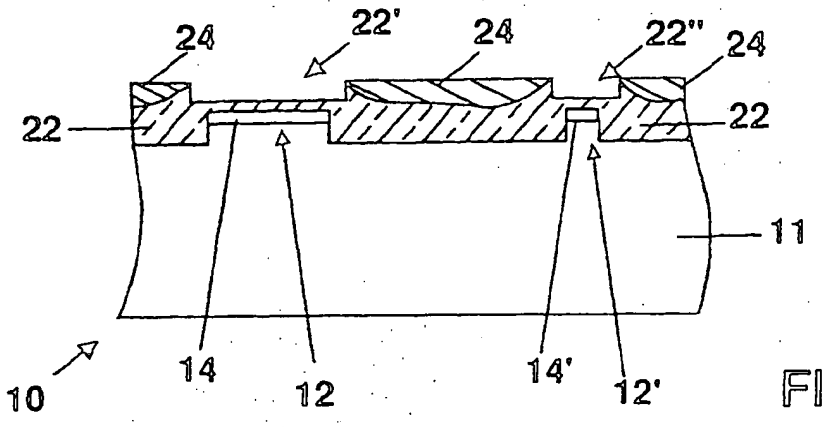


FIG. 1E

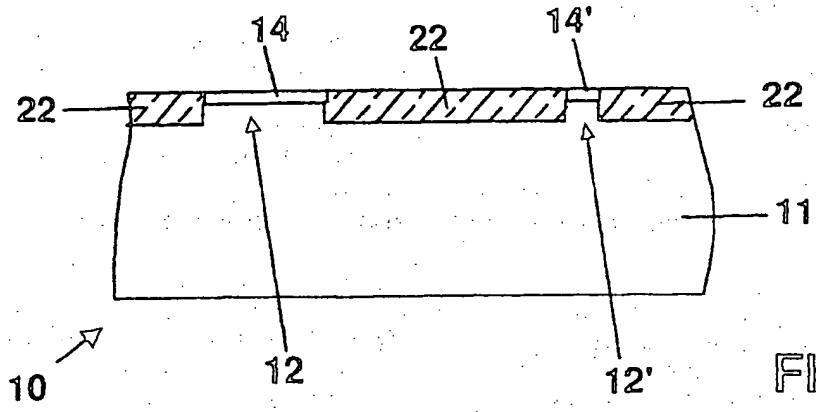


FIG. 1G

## Description

### Field of the Invention

This invention relates to semiconductor devices and more particularly to shallow trench isolation in self-aligned FET devices.

### Description of Related Art

Conventional STI (Shallow Trench Isolation) planarization methods require a planarization mask, extensive measurements, and wafer-to-wafer process customization.

Maskless STI Planarization using Self-Aligned Polysilicon process allows STI to be planarized without a planarization mask, with minimal measurements, without the need for wafer to wafer customization and can be designed to be completely ground rule compatible with a gate conductor stack Fill technology.

United States patent No. 5,173,439 of Dash et al for "Forming Wide Dielectric-Filled Isolation Trenches In Semiconductors" shows isolation trenches formed in pad silicon nitride/Si, followed by a silicon oxide layer, followed by a polysilicon layer, followed by Chemical Mechanical Polishing (CMP); followed by silicon oxide RIE (Reactive Ion Etching); followed by CMP down to a pad silicon nitride layer.

U.S. patent No. 5,504,033 of Bajor et al for "Method for Forming Recessed Oxide Isolation Containing Deep And Shallow Trenches" describes in a fifth embodiment, after isolation trenches are dug into silicon nitride over silicon oxide over silicon, the trenches along with horizontal surfaces are first layered with silicon oxide, then sequentially a polysilicon layer; is followed by CMP. This reference appears not to address selective RIE partial silicon oxide etch over pad areas.

United States patent No. 5,411,913 of Bashir et al for "Simple Planarized Trench Isolation and Field Oxide Formation using Poly-silicon" describes a process where after trenches are dug into pad silicon oxide/silicon nitride and into silicon; a layer of silicon oxide is deposited, followed by a layer of polysilicon, followed by RIE etch back to planarize. This reference appears not to address CMP polishing down to the silicon oxide layer and selective RIE partial silicon oxide etching over pad areas.

United States patent No. 5,492,858 of Bose et al for "Shallow Trench Isolation Process Method for High Aspect Ratio Trenches" describes a process in which, after isolation trenches are dug through the pad silicon oxide/silicon nitride into silicon, a layer of silicon oxide is deposited and CMP etched back to silicon nitride to provide a planar surface for "active mesa sites." Bose et al. does not address deposition of polysilicon on a silicon oxide layer; CMP polishing down to the silicon oxide layer; and selective RIE partial silicon oxide etching over pad areas.

United States patent No. 5,494,857 of Cooperman et al for "Chemical Mechanical Planarization of Shallow Trenches in Semiconductor Substrates" describes a process where, after trenches are dug in through pad silicon nitride/silicon oxide, a first silicon oxide layer is deposited, followed by a first silicon etch stop layer, followed by a second silicon oxide layer; followed by a CMP down to pad silicon nitride.

United States patent No. 5,252,517 of Blalock et al for "Method Of Conductor Isolation From A Conductive Contact Plug", describes a process where, after transistors are completed, a "planarizing insulator layer" is deposited and contact vias are etched down to diffusion areas and filled with polysilicon.

United States patent No. 5,358,884 of Violette for "Dual Purpose Contact Collector Contact and Isolation Scheme for Advanced BICMOS Processes" shows trenches are dug through silicon nitride into silicon. Silicon oxide is deposited upon the silicon nitride, and CMP is done down to silicon nitride to create a "plurality of mesas."

FIG. 3 shows an isolation region of a prior art MOSFET device 60 with a doped silicon semiconductor substrate 62 on which an STI region 72 has been formed. Above the STI region is formed a gate conductor stack 74 of fill layers comprising a polysilicon layer 64, a silicide layer 68, and a silicon nitride gate insulator layer 70.

See J.-Y. Cheng, T.F. Lei, T.S. Chao, D.L.W.Yen, B.J. Jin, and C. J. Lin "A Novel Planarization of Oxide-Filled Shallow-Trench Isolation" J. Electrochem. Soc., Vol. 144, No.1, (Jan., 1997) pp. 315-320.

### DISCLOSURE OF THE INVENTION

Maskless STI (MSTI) Planarization for gate conductor Fill Technology is accomplished by designing the AA (active area) mask with dummy active silicon mesas within the holes of gate conductor punch-holes. These dummy active silicon mesas are designed with the same ground rules as the rest of the chip.

Dash et al discusses STI planarization using polysilicon but differs from the present invention in several ways with respect to the level of the silicon oxide fill and the level of the polysilicon. The silicon oxide RIE used after polysilicon CMP does not include the required break-thru step and stops on the silicon nitride instead of in the silicon oxide. Both the break-thru step and having the RIE stop in the silicon oxide were found to be essential in creating a manufacturable process

None of the patents discussed above describes the active area (AA) fill concept.

In accordance with this invention, a method is provided for manufacture of a semiconductor FET device employing a Shallow Trench Isolation (STI) comprising the steps of: providing a doped silicon semiconductor substrate coated with a pad structure on the surface thereof; forming raised active silicon device areas and dummy active silicon mesas capped with pad structures from the doped silicon semiconductor substrate and the pad structure; depositing a conformal blanket silicon oxide layer on the device with conformal projections above the mesas; depositing a conformal blanket sacrificial layer on the blanket silicon oxide layer with additional conformal projections above the mesas; planarizing the blanket sacrificial layer to remove the additional conformal projections until the silicon oxide layer is exposed over the pad structures; selectively RIE etching the conformal silicon oxide layer partially over the mesas; and planarizing the conformal blanket silicon oxide layer.

Preferably, the pad structures are composed of silicon nitride; or the pad structures are composed of a lower layer of silicon oxide capped with an upper layer of silicon nitride.

It is also preferred that after the second chemical mechanical polishing, the pad structures are stripped away from the device and then gate oxide layers are formed above the surfaces of the substrate exposed by stripping away the pad structures.

In addition, after formation of the gate oxide layer P-wells and N-wells are formed in the substrate beneath the gate oxide layer and the silicon oxide layer.

Following formation of the wells there is a step of blanket deposition of a gate conductor layer composed of a polysilicon sublayer and a silicide sublayer upon the device followed by blanket deposition of a dielectric layer, followed by patterning and etching of windows down to active device areas and dummy areas in the substrate followed by the step of formation of FET devices and dummy devices by ion implantation of a dose of source/drain dopant ions into the active device areas and the dummy areas in the P-wells and the N-wells.

In accordance with another aspect of this invention, a Shallow Trench Isolation (STI) semiconductor FET device comprises a doped silicon semiconductor substrate with raised active silicon device areas and dummy active silicon mesas capped with a gate oxide layer and the substrate being coated with a planarized silicon oxide layer elsewhere. There are P-wells and N-wells formed in the substrate beneath the gate oxide layers and the silicon oxide layer, and a gate conductor layer and a dielectric layer formed over the gate oxide layers and the silicon oxide layer patterned into active devices, and dummy devices.

In accordance with another aspect of this invention, a Shallow Trench Isolation (STI) semiconductor FET device comprises a doped silicon semiconductor substrate with raised active silicon device areas and dummy active silicon mesas capped with a gate oxide layer and the substrate being coated with a planarized silicon oxide layer elsewhere, a gate conductor layer and a dielectric layer formed over the gate oxide layers, and polysilicon and dielectric layers being formed above the silicon oxide layer which are then patterned into dummy devices surrounding the mesas providing a pattern of punch hole vias.

Preferably, the pad structure is stripped from the device and a gate oxide layer is formed above the surface of the substrate exposed as the pad structure is stripped away.

Preferably, FET devices with gate structure are formed on the surface of the device with gate conductor structures and dummy structures formed on the surface of the planar silicon oxide layer.

"Gate Conductor (GC) stack Fill" over trenches, and etch of the fill to produce vias for vertical contacts to diffusion areas on active sites.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIGS. 1A-1O illustrate a process of manufacturing a Shallow Trench Isolation (STI) device in accordance with this invention.

FIGS. 2A-2G illustrate a process of manufacturing a Shallow Trench Isolation (STI) device in accordance with this invention with deep trench capacitor structures.

FIG. 3 shows an isolation region of a prior art MOSFET device.

FIG. 4 shows a perspective view of the device in accordance with this invention with a dummy area in which the vias reach down into dummy regions where no active devices have been formed. The structure is otherwise the same as the device described in FIGS. 1A-1O.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGS. 1A-1O illustrate a process of manufacturing a Shallow Trench Isolation (STI) device 10 in accordance with this invention.

FIG. 1A shows the device 10 in an early stage of manufacture. The device 10 is formed on a P-doped silicon substrate 11 upon which pad silicon dioxide/silicon nitride pad layer segments 14/14' have been formed. In the pad layers segments 14/14' the silicon dioxide layer has a thickness from about 5nm to about 15nm and the silicon nitride layer has a thickness from about 100nm to about 150nm. The active area mask 15/15' has been formed on the surface of silicon nitride layer segments 14/14' to protect the pad silicon dioxide/silicon nitride pad layer segments 14/14' and the silicon mesas 12/12' formed from the substrate 11 beneath the mask 15/15' during etching of the pad layers 14/14' and etching shallow trenches 9/9'/9" in substrate 11 to a depth H below the surface of the pad layer segments 14/14'. The depth H is from about 350nm to about 480nm below the upper surface of the pad layer segments 14/14'.

FIG 1B shows the device 10 of FIG. 1A after the mask 15/15' has been stripped away from the device 10, leaving the substrate 11 with the raised (mesa) active areas 12, 12' covered with pad structures 14, 14'. The space between the pad structures 14. 14' is a width W from about 250nm to about 250µm.

FIG. 1C shows the device 10 of FIG. 1B after deposition of a silicon dioxide layer 22 (having a thickness from about 480nm to about 560nm) on the device 10 covering the shallow trenches 9/9'/9" and the pad layer segments 14/14' and the mesas 12/12' Next the silicon dioxide layer 22 on device 10 is covered by deposition of a blanket polysilicon layer 24 on silicon oxide layer 22. Layer 24 has a thickness from about 400nm to about 480nm.

FIG. 1D shows the device 10 of FIG. 1C after CMP (Chemical Mechanical) Polishing of blanket polysilicon layer 24 down to those portions of silicon dioxide layer 22 which are exposed because they overlie the remaining portions of the pad layer segments 14/14' above the mesas 12/12'.

FIG. 1E shows the device 10 of FIG. 1D after selective RIE partial etching of the exposed surface of the silicon dioxide layer 22 forming hollows 22' and 22" above the pad layer segments 14/14' above the mesas 12/12'. The etching removes a thickness from about 320nm to about 470nm of the silicon dioxide layer 22 over the remaining areas of pad layer 14/14'.

FIG. 1F shows the device 10 of FIG. 1E after removal of the remainder of the polysilicon layer 24 with a selective etchant which removes the polysilicon layer 24 while leaving the silicon dioxide structure 22 with hollows 22'/22" intact. In this case a thickness from about 20nm to about 430nm of polysilicon layer 24 is removed.

FIG. 1G shows the device 10 of FIG. 1F after a CMP process was used for about 50 seconds to about 70 seconds planarizing silicon dioxide layer 22 and clearing away the silicon nitride portion of pad layer 14/14'. Thus the CMP process leaves the surface of device 10 as a planarized surface of silicon dioxide layer 22.

FIG. 1H shows the device 10 of FIG 1G after the silicon nitride and the silicon dioxide layers of the pad layer 14/14' have been stripped from device 10 leaving openings 24/24' in planar silicon dioxide layer 22 down to the surfaces of the mesas 12/12' exposed between the remaining portions of the silicon dioxide layer 22.

FIG. 1I shows the device 10 of FIG. 1H after "gate" sacrificial silicon dioxide gate segments 30/30' about 12.5nm thick have been formed above the mesas 12/12' by the conventional process of oxidation of the exposed surface of the substrate 11. Then $V_T$ implants are made through the sacrificial silicon dioxide gate segments 30/30' into the substrate 11.

In addition, an N-well mask 31" has been formed over the device 11 with a N-well window 31'" over the sacrificial silicon dioxide gate segments 30/30' through which N type dopant ions 31' are ion implanted into the surface of substrate 11 below the gate segment 30 to form an N-well 31.

FIG. 1J shows the device 10 of FIG. 1I after N-well mask 31" has been stripped away and a P-well mask 32" has been formed over the device 11 with a P-well window 32'" over the sacrificial silicon oxide gate segment 30' through which P type dopant ions 32' are ion implanted into the surface of substrate 11 below the gate segment 30 forming a P-well region 32.

FIG. 1K shows the device 10 of FIG. 1J after the sacrificial silicon oxide gate segments 30/30' have been stripped away by etching which also thins the silicon dioxide layer 22 to be coplanar with the surface of device 11. Then conventional gate silicon oxide (gate oxide) layer segments 38/38' (about 10nm thick) are formed on the surface of the mesas 12/12' within the recently enlarged openings 24/24'.

FIG. 1L shows the device 10 of FIG. 1K after the planar oxide layer 22' and the gate oxide layer segments 38/38' have been coated with a doped polysilicon layer 40 preferably about 100nm thick, with a thickness range from about 50nm to about 100nm. Polysilicon layer 40 is coated with a silicide layer 42 preferably a tungsten silicide layer about 80nm thick. with a thickness range from about 50nm to about 200nm. Tungsten silicide layer 42 is coated with a silicon dioxide or silicon nitride gate insulator layer 44 preferably about 280nm thick, with a thickness range from about 200nm to about 400nm.

Next, the device is coated with a photoresist gate stack mask 46 with openings 48A, 48B therethrough over the ends of gate oxide layer segment 38 N-well and opening 48C therethrough over P-well 36.

FIG. 1M shows the device 10 of FIG. 1L after the introduction of RIE etchant through openings 48A, 48B, and 48C down through gate insulator layer 44 etching openings 50A, 50B, and 50C therein extending down through tungsten silicide layer 42 and doped polysilicon layer 40 to expose the surface of the gate oxide layer segments 38/38' leaving a gate conductor stack 51 over N-well 34 with source/drain windows on either side and a dummy window 50C exposing

the P-well for ion implanting subsequently.

FIG. 1N shows the device 10 of FIG. 1M after ion implanting the P+ dopant source/drain regions 56S/56D below the silicon oxide segment 38 self-aligned with the gate conductor stack 51.

FIG. 1O shows the device 10 of FIG. 1N after ion implanting the P+ dopant regions 58.

By designing dummy active silicon mesas in STI regions within the gate conductor stack by filling punch-hole areas, a maskless STI (MSTI) planarization process previously can be realized on products incorporating STI and gate conductor stack Fill technologies.

FIGS. 2A-2G illustrate a process of manufacturing a Shallow Trench Isolation (STI) device 10 in accordance with this invention with deep trench capacitor structures 16. Corresponding structures in FIGS. 2A-2G are the same as those in FIGS. 1A-1G and the descriptions thereof apply to a device 10 which includes the deep trench capacitor structures 16 initially at the beginning of the process of manufacture.

FIG. 4 shows a perspective, sectional view of a portion of the device 10 in accordance with this invention with a dummy area in which the vias 54 reach down into dummy regions where no active devices have been formed. The structure is otherwise the same as the device described in FIGS. 1A-1O. The device 10 is formed on the P-doped silicon substrate 11 upon which silicon mesas 12 have been formed from the substrate 11 between the recesses therein containing the shallow trenches filled with the silicon oxide regions 22 upon which dummy gate conductor stacks of polysilicon layer 40, silicide layer 42 and the silicon dioxide or silicon nitride dielectric layer 44 have been formed. Between the dummy conductor stacks are the vias 54 (punch holes) which extend down to the top of the mesas 12.

Maskless STI Planarization Using Self-Aligned Polysilicon.

For the ideally scalable ULSI CMOS device, process control of the isolation technology is crucial. Device isolation needs to provide an abrupt active-to-isolation transition with sufficient isolation depth and to provide a planar wafer surface. This must be achieved with a wide process window at a low cost.

Several alternative planarization techniques have been proposed. For example, LOCOS is inexpensive but suffers from insulator thinning at narrow dimensions, bird's beak formation, field-implant encroachment, and creates significant wafer topography. Poly-Buffered LOCOS and Polyencapsulated LOCOS improved the bird's beak formation but still result in a narrow channel effect that increases device Vts.

Shallow Trench Isolation (STI) provides an abrupt active-to-isolation transition without bird's beak formation with a minimum impact on device characteristics or topography. However, the process often requires extensive measurements and wafer to wafer process customization to control, i.e., a resist planarization mask used for fabrication of a 16Mb DRAM, and has a higher cost than LOCOS based methods.

A manufacturable STI planarization process using Self-Aligned polysilicon and a planarization mask provides a stable and reliable process with a robust process window. It does not require extensive inline measurements or wafer to wafer process customization to control.

The Self-Aligned Poly-silicon planarization process can be greatly simplified by use of mesas of active silicon within the STI regions in accordance with this invention. This allows the planarization mask, CMP stop silicon oxide layer deposition, and the CMP stop silicon oxide layer etch to be completely eliminated. This is compatible with a gate conductor stack with fill technology by using a 'punch-hole' gate conductor stack mask. This allows large area STI regions to have active silicon mesas placed within the gate conductor stack-fill 'punch-hole' areas, thus creating additional polish stop areas to prevent CMP dishing in the STI regions during planarization.

Maskless STI Planarization Using Self-Aligned Polysilicon

Process

1. Substrates start with an STI of depth "H" with maximum width W. "H" depends on device design requirements. "W" depends on planarization distance of CMP pad used for polishing sacrificial polysilicon (~30-50 μm for an IC1000 CMP Pad);

2. STI shapes are designed to have active silicon mesas placed within the gate conductor stack-Fill "punch-hole" areas;

3. Deposition of silicon oxide layer to be planarized of thickness "H" + 25% Ox; over initial pad structure (e.g. silicon nitride);

4. Deposition of polysilicon sacrificial layer of thickness "H" over silicon oxide layer.

5. CMP polysilicon layer stopping on silicon oxide layer;

6. Using a combination of non-selective & selective silicon oxide/polysilicon RIE, etch the silicon oxide over the initial pad structure to be coplanar with the top of the silicon oxide in the large STI areas. The RIE will leave a thin layer of polysilicon over the STI regions;

7. Selectively strip remaining polysilicon.

8. CMP remaining silicon oxide down to initial pad structure.

## Supporting Data

## Cost of Ownership of STI Planarization Using Self-Aligned Poly-silicon

| | | | | | | MASKED | | MASKLESS | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SEQ | MOD | | EX | PROCESS | DESCRTOOL | Tput | | DESCRTOOL | Tput | |
| | | | | | | WF/HR | $ | | WF/H | $ |
| 2110 | 020 | ST | 1 | LITHO (AA IT RX) | AA 10 | 25 | 17.83 | AA 10 | 25 | 17.83 |
| 2111 | 020 | ST | | INSPECT LITHO | 140 | 75 | 1.34 | 140 | 75 | 1.34 |
| 2112 | 020 | ST | | MEAS O L | 160 | 75 | 0.96 | 160 | 75 | 0.96 |
| 2113 | 020 | ST | | MEAS LINEWIDTH | 150 | 250 | 0.58 | 150 | 250 | 0.58 |
| 2130 | 020 | ST | | ETCH ST | 1230 | 10 | 15.21 | 1230 | 10 | 15.21 |
| 2131 | 020 | ST | | PLASMA STRIP | 1200 | 30 | 1.84 | 1200 | 30 | 1.84 |
| 2134 | 020 | ST | | MEAS AFM THICKNESS | 210 | 150 | 0.47 | 210 | 150 | 0.47 |
| 2150 | 020 | ST | | CLEAN SP STRIP | 1400 | 75 | 1.46 | 1400 | 75 | 1.46 |
| 2153 | 020 | ST | | MEAS LINEWIDTH | 150 | 250 | 0.58 | 150 | 25 | 0.58 |
| 2170 | 020 | ST | | CLEAN S P STRIP | 1400 | 75 | 1.46 | 1400 | 75 | 1.46 |
| 2189 | 020 | ST | | PC IT OX | 1410 | 125 | 1.40 | 1410 | 125 | 1.40 |
| 2190 | 020 | ST | | OX ET SAC | 1180 | 20 | 4.61 | 1180 | 20 | 4.61 |
| 2194 | 020 | ST | | MEAS THICKNESS | 200 | 300 | 0.26 | 200 | 300 | 0.26 |
| 2100 | 020 | ST | | NITR LINER | | | | | | |
| 2104 | 020 | ST | | MEAS THICKNESS | | | | | | |
| 2210 | 020 | ST | | TEOS AA | 1120 | 10 | 12.95 | 1120 | 10 | 12.95 |
| 2214 | 020 | ST | | MEAS THICKNESS | 200 | 300 | 0.26 | 200 | 300 | 0.26 |
| 2230 | 020 | ST | | POLY PETRI NITRIDE | 1110 | 30 | 3.64 | 1110 | 30 | 3.64 |
| 2234 | 020 | ST | | MEAS THICKNESS | 200 | 300 | 0.26 | 200 | 300 | 0.26 |
| 2250 | 020 | ST | | DEP OX | 1300 | 20 | 11.68 | | | |
| 2254 | 020 | ST | | MEAS THICKNESS | 200 | 300 | 0.26 | | | |
| 2510 | 020 | ST | 1 | LITHO (AC.AB) | AC 20 | 30 | 11.00 | | | |
| 2511 | 020 | ST | | INSPECT LITHO | 140 | 75 | 1.34 | | | |
| 2512 | 020 | ST | | MEAS. O L | 160 | 75 | 0.96 | | | |
| 2513 | 020 | ST | | MEAS. LINEWIDTH | 150 | 250 | 0.58 | | | |
| 2520 | 020 | ST | | BAKE RESIST | | | | | | |
| 2530 | 020 | ST | | RESIST PLANARIZE | | | | | | |
| 2531 | 020 | ST | | INSPECT RESIST | | | | | | |
| 2537 | 020 | ST | | BAKE RESIST 2 | | | | | | |
| 2540 | 020 | ST | | ETCH AB | | | | | | |
| 2544 | 020 | ST | | MEAS. THICKNESS | | | | | | |
| 2550 | 020 | ST | | ETCH REWORK AB | | | | | | |
| 2551 | 020 | ST | | PLASMA STRIP | | | | | | |
| 2552 | 020 | ST | | INSPECT STRIP | | | | | | |
| 2554 | 020 | ST | | MEAS. THICKNESS | | | | | | |
| 2560 | 020 | ST | | ETCH PETRI MASK OX | 1410 | 125 | 1.40 | | | |
| 2570 | 020 | ST | | CLEAN SP STRIP - 100:1 DHF | | | | | | |
| 2590 | 020 | ST | | CMP IT | 940 | 20 | 7.17 | 940 | 20 | 7.17 |
| 2594 | 020 | ST | | MEAS. AFM | | | | | | |
| 2597 | 020 | ST | | BRUSH CLN | 970 | 30 | 3.25 | 970 | 30 | 3.25 |
| 2599 | 020 | ST | | CLEAN HALING AB | 1410 | 125 | 1.40 | 1410 | 125 | 1.40 |
| 2610 | 020 | ST | | ETCH PETRI BULK OX | 1230 | 20 | 8.11 | 1230 | 20 | 8.11 |
| 2620 | 020 | ST | | CLEAN 100 1 - DHF 6 KOH | | | | | | |
| 2625 | 020 | ST | | PC ANNEAL - SP HUANG A18 | 1410 | 125 | 1.40 | 1410 | 125 | 1.40 |
| 2630 | 020 | ST | | ANNEAL AA DENS | 1150 | 20 | 4.38 | 1150 | 20 | 4.38 |
| 2634 | 020 | ST | | MEAS. AFM | | | | | | |
| 2650 | 020 | ST | | CMP OX | 960 | 20 | 8.17 | 960 | 20 | 8.17 |
| 2653 | 020 | ST | | MEAS. THICKNESS | 200 | 300 | 0.26 | 200 | 300 | 0.26 |
| 2654 | 020 | ST | | MEAS. AFM | 210 | 150 | 0.47 | 210 | 150 | 0.47 |
| 2657 | 020 | ST | | BRUSH CLN | 970 | 30 | 3.25 | 970 | 30 | 3.25 |
| 2658 | 020 | ST | | INSPECT CMP | 140 | 75 | 1.34 | 140 | 75 | 1.34 |
| 2659 | 020 | ST | | CLEAN HAUNG AB | 1410 | 125 | 1.40 | 1410 | 125 | 1.40 |
| 2729 | 020 | ST | | P C IT DENS ANNEAL | | | | | | |
| 2730 | 020 | ST | | ANNEAL IT DENS | | | | | | |
| 2740 | 020 | ST | | STRIP NITRIDE | 1410 | 36 | 3.45 | 1410 | 36 | 3.45 |
| 2741 | 020 | ST | | INSP. STRIP | 140 | 75 | 1.34 | 140 | 75 | 1.34 |
| 2748 | 020 | ST | | CLEAN | | | | | | |
| 2749 | 020 | ST | | P C 100 DHF - HUANG A 8 | 1420 | 66 | 1.94 | 1420 | 66 | 1.94 |
| 2750 | 020 | ST | | OX TG SAC | 1180 | 20 | 4.61 | 1180 | 20 | 4.61 |
| 2754 | 020 | ST | | MEAS. THICKNESS | 200 | 300 | 0.26 | 200 | 300 | 0.26 |
| TOTAL W/O KV | | | | | | | $144.53 | | | $117.31 |

The cost has been calculated to decrease from about $145 to about $117 for the STI planarization module using MSTI.

Operations Summary

Much development effort was invested in creating a manufacturable STI planarization process using self-aligned polysilicon for this process. Data was collected and analyzed from hundreds of integrated product lots showing that the method of this invention for STI planarization creates a stable process with a large process window.

Simplifying the self-aligned polysilicon STI planarization process by eliminating a planarization mask allows the polysilicon CMP stop silicon oxide layer and polysilicon CMP stop silicon oxide etch processes to be eliminated also.

By designing active silicon mesas within large STI regions (within the gate conductor stack-Fill punch-hole areas in a gate conductor stack-Fill technology) and limiting the largest STI width to the planarization distance of CMP pad used for polishing the sacrificial polysilicon (~30-50 μm for an IC1000 CMP pad), MSTI can be easily implemented.

There is a gate conductor (GC) stack with fill over trenches, and the fill is etched to produce vias for vertical contacts to diffusion areas on active sites.

## Claims

1. A method of manufacture of a semiconductor FET device (10) employing a Shallow Trench Isolation (STI), the method comprising the steps of:

   a) providing a doped silicon semiconductor substrate (11) coated with a pad structure (14) on the surface thereof,

   b) forming raised active silicon device areas and dummy active silicon mesas (12, 12') capped with pad structures from said doped silicon semiconductor substrate and said pad structure,

   c) depositing a conformal blanket silicon oxide (22) layer on b) above with conformal projections above said mesas,

   d) depositing a conformal blanket sacrificial layer (24) on said blanket silicon oxide layer with additional conformal projections above said mesas,

   e) planarizing said blanket sacrificial layer (24) to remove said additional conformal projections until said silicon oxide layer is exposed over said pad structures,

   f) selectively RIE etching said conformal silicon oxide layer (22) partially, over said mesas, and

   g) planarizing said conformal blanket silicon oxide layer (22).

2. A method as claimed in claim 1 wherein said planarizing steps (e) and (g) comprise performing chemical mechanical polishing.

3. A method as claimed in claim 1 or claim 2 wherein said pad structures (14) are composed of silicon nitride used as an etch stop in planarizing said silicon oxide layer (22) into a planar silicon oxide layer.

4. A method as claimed in claim 1 or claim 2 wherein said pad structures (14) are composed of a lower layer of silicon oxide capped with an upper layer (14) of silicon nitride using said silicon nitride in said pad structure as an etch stop in planarizing said silicon oxide layer (22) into a planar silicon oxide layer.

5. A method as claimed in claim 2 wherein the method further comprises the step of, after said chemical mechanical polishing in step (g), stripping away said pad structures from said device (10) and then forming gate oxide layers above the surfaces of said substrate exposed by stripping away said pad structures.

6. A method as claimed in claim 5 wherein after formation of said gate oxide (38), layer P-wells (36) and N-wells (34) are formed in said substrate beneath said gate oxide layer and said silicon oxide layer (22).

7. A method as claimed in claim 6 wherein following formation of said wells (36, 34) there is a step of blanket deposition of a gate conductor layer upon said device (10) followed by blanket deposition of a dielectric layer (40), followed by patterning and etching of windows down to active device areas and dummy areas in said substrate (11) followed



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by the step of formation of FET devices and dummy devices by ion implantation (56, 58) of a dose of source/drain dopant ions into said active device areas and said dummy areas in said P-wells (36) and said N-wells (34).

**8.** A method as claimed in claim 6 wherein following formation of said wells (36, 34) there is a step of blanket deposition of a gate conductor layer composed of a polysilicon sublayer (40) and a silicide sublayer (42) upon said device (10) followed by blanket deposition of a dielectric layer (44), followed by patterning and etching of windows down to active device areas and dummy areas in said substrate followed by the step of formation of FET devices and dummy devices by ion implantation (56, 58) of a dose of source/drain dopant ions into said active device areas and said dummy areas in said P-wells (36) and said N-wells (34).

**9.** A Shallow Trench Isolation (STI) semiconductor FET device (10) comprising:

a doped silicon semiconductor substrate (11) with raised active silicon device areas and dummy active silicon mesas (12, 12') capped with a gate oxide layer (38) and said substrate being coated with a planarized silicon oxide layer (22) elsewhere,

P-wells (36) and N-wells (34) formed in said substrate under said gate oxide layers and said silicon oxide layer,

a gate conductor layer and a dielectric layer (44) formed over said gate oxide layers and said silicon oxide layer patterned into active devices, and dummy devices.

**10.** A Shallow Trench Isolation (STI) semiconductor FET device (10) comprising:

a doped silicon semiconductor substrate (11) with raised active silicon device areas and dummy active silicon mesas (12, 12') capped with a gate oxide layer (38) and said substrate being coated with a planarized silicon oxide layer (22) elsewhere,

a gate conductor layer and a dielectric layer (44) formed over said gate oxide layers,

polysilicon (40) and dielectric layers being formed above said silicon oxide layer which are then patterned into dummy devices surrounding said mesas providing a pattern of punch hole vias.

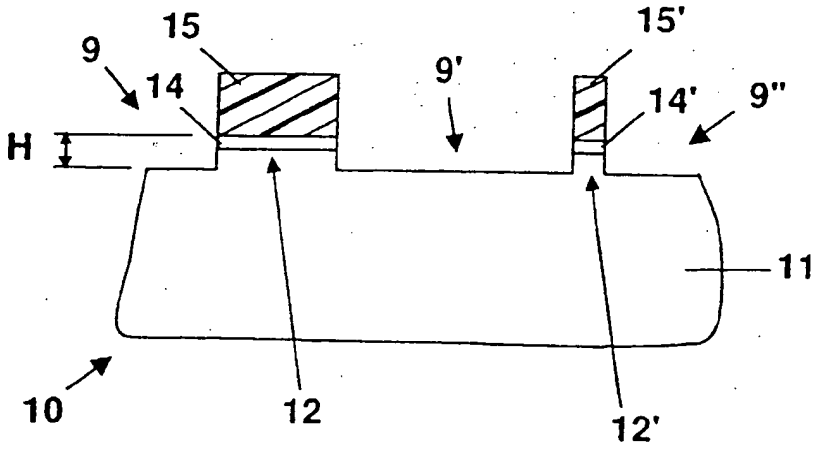



FIG. 1A

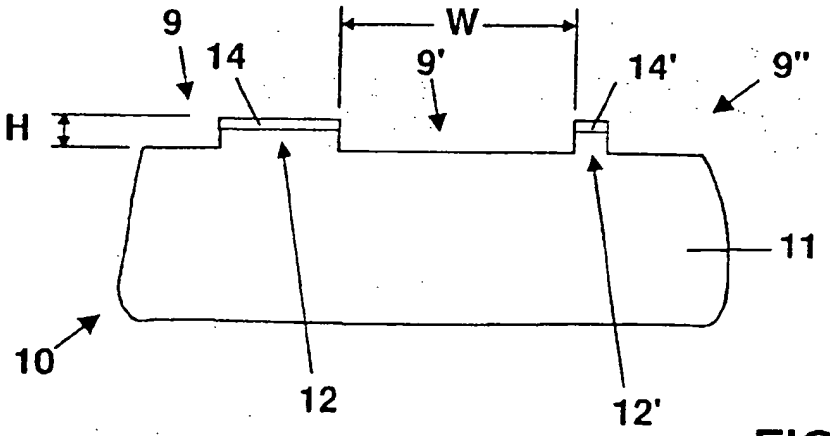



FIG. 1B

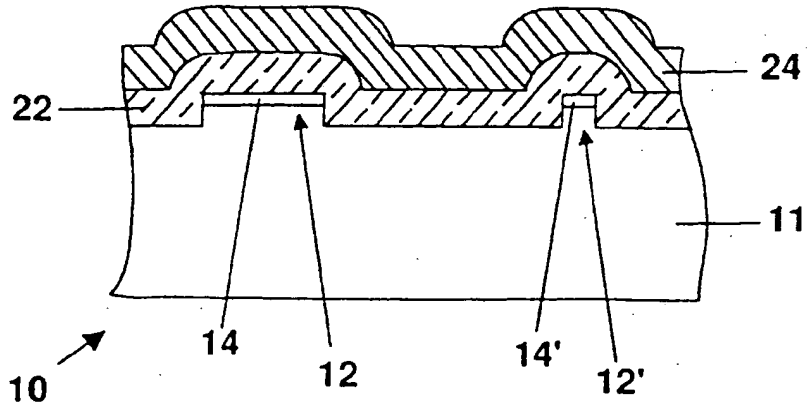



FIG. 1C

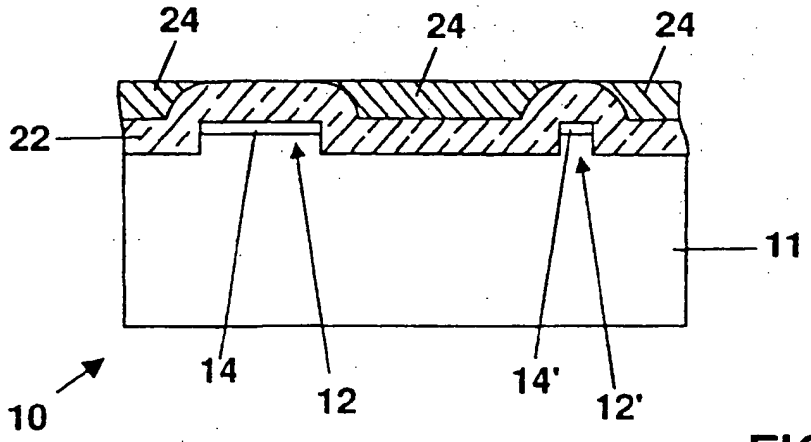



FIG. 1D

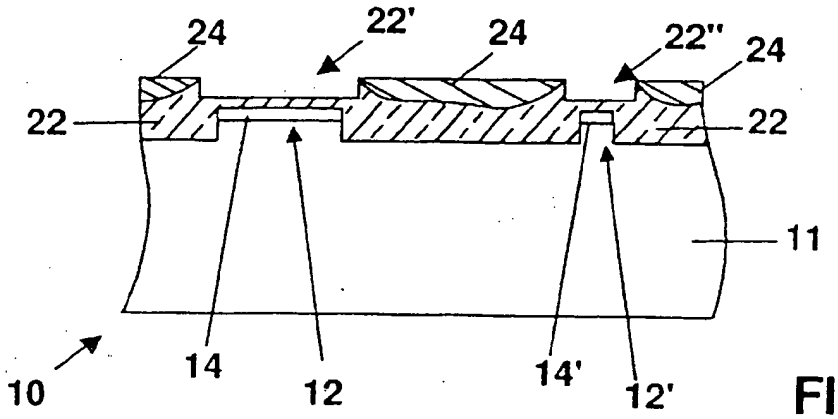



FIG. 1E

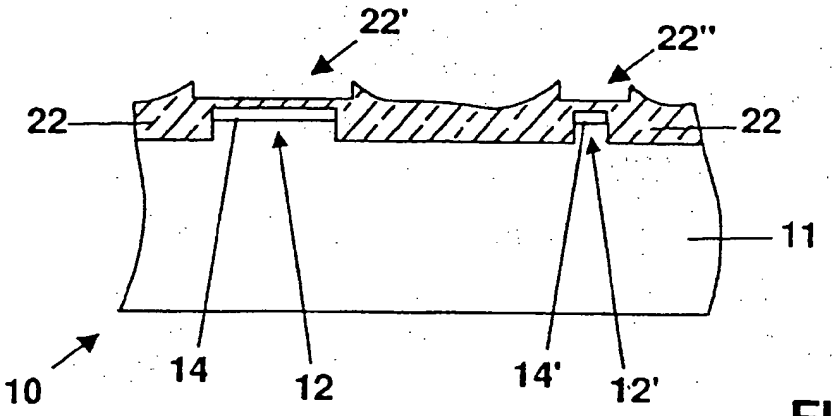



FIG. 1F

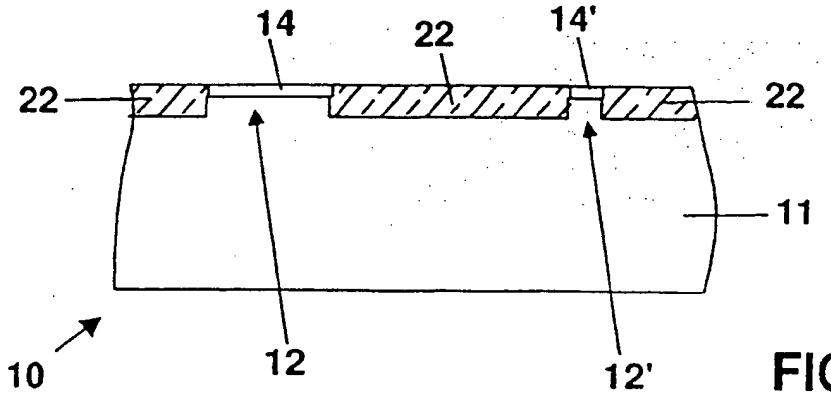



FIG. 1G

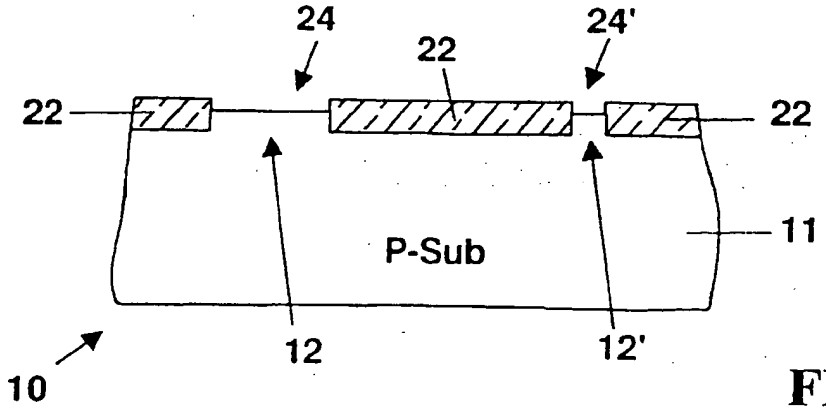



FIG. 1H

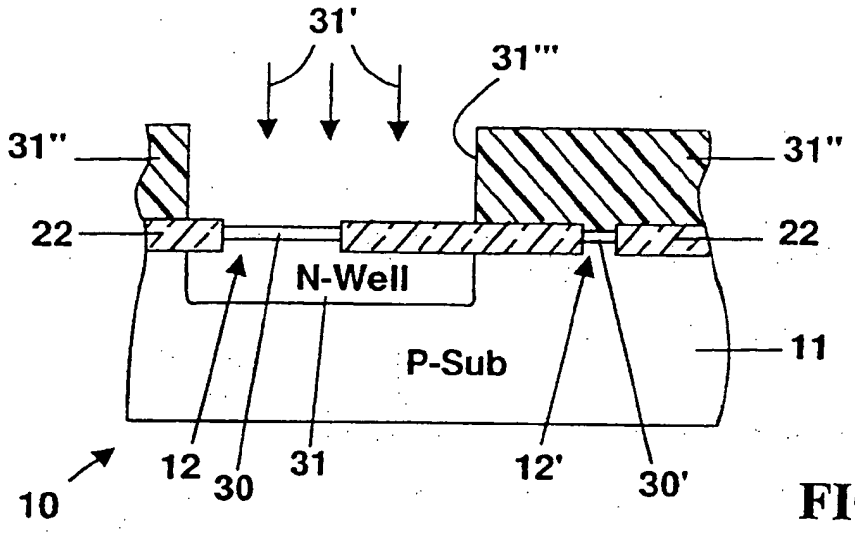



FIG. 1I

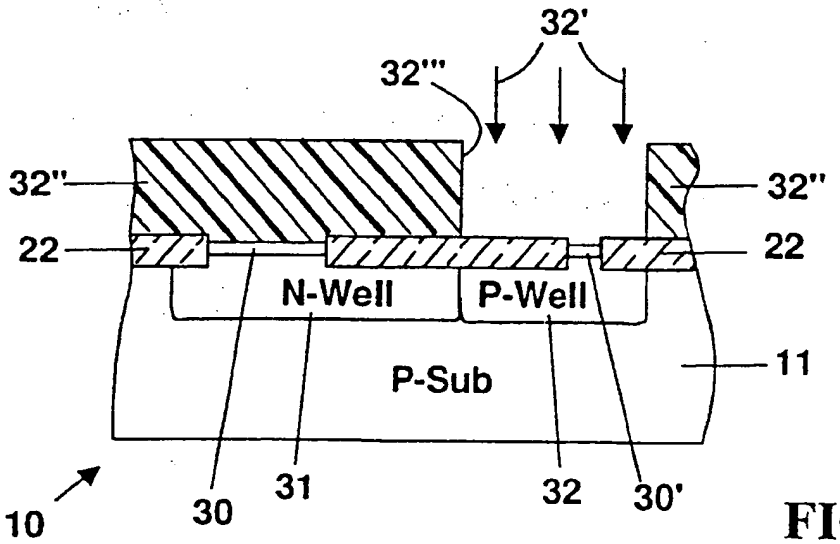



FIG. 1J

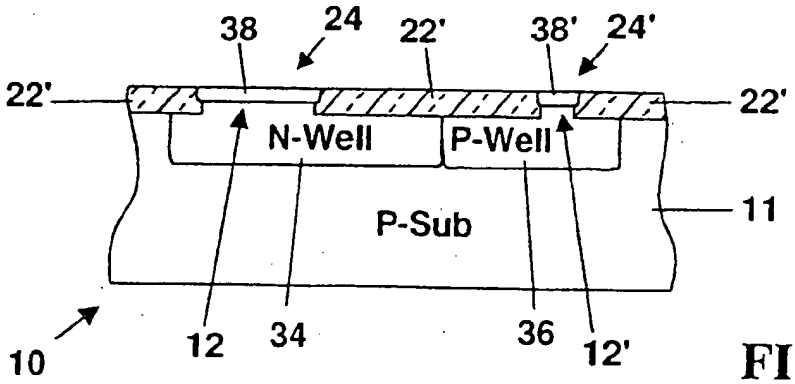



FIG. 1K

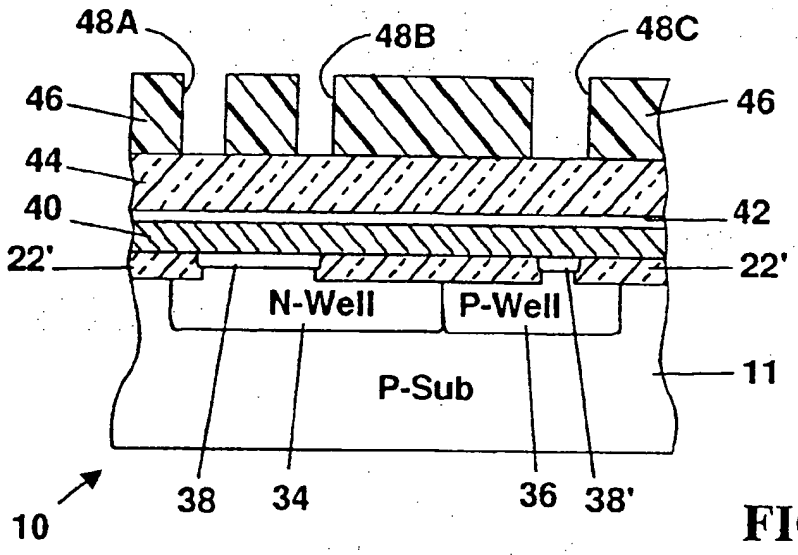



FIG. 1L

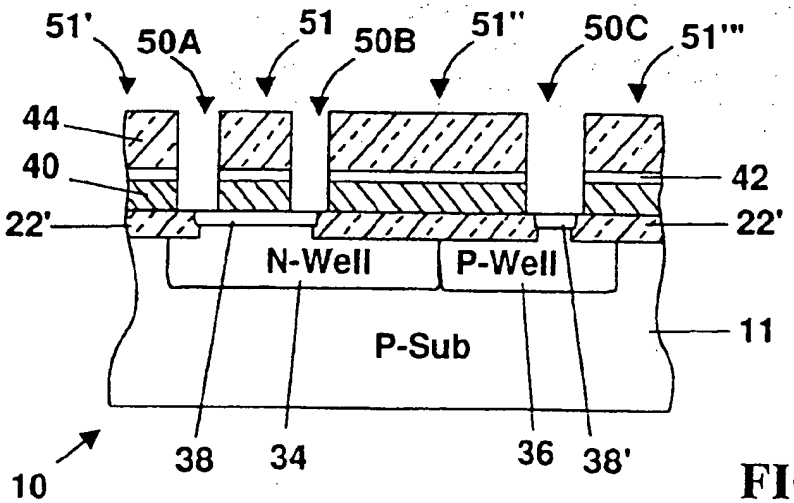



FIG. 1M

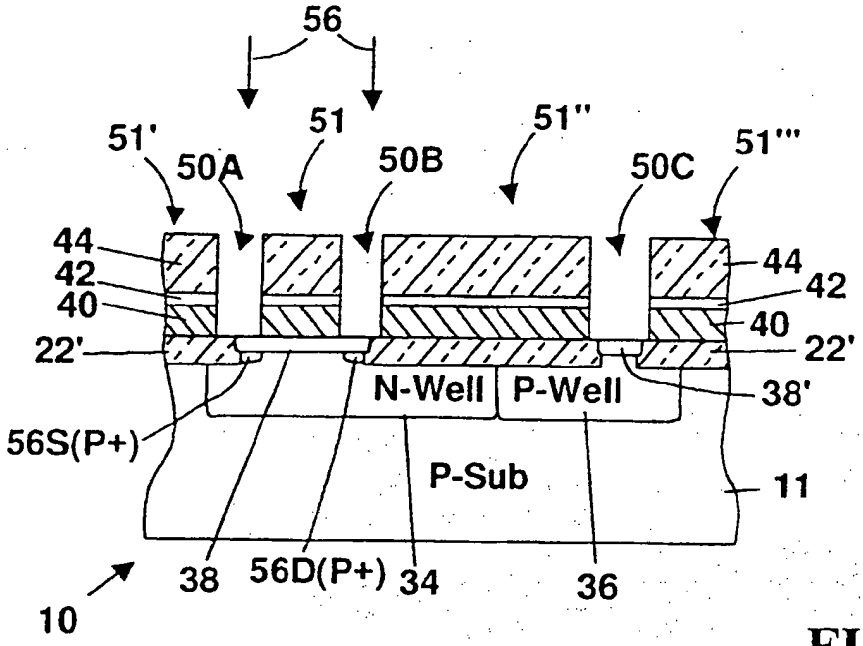



FIG. 1N

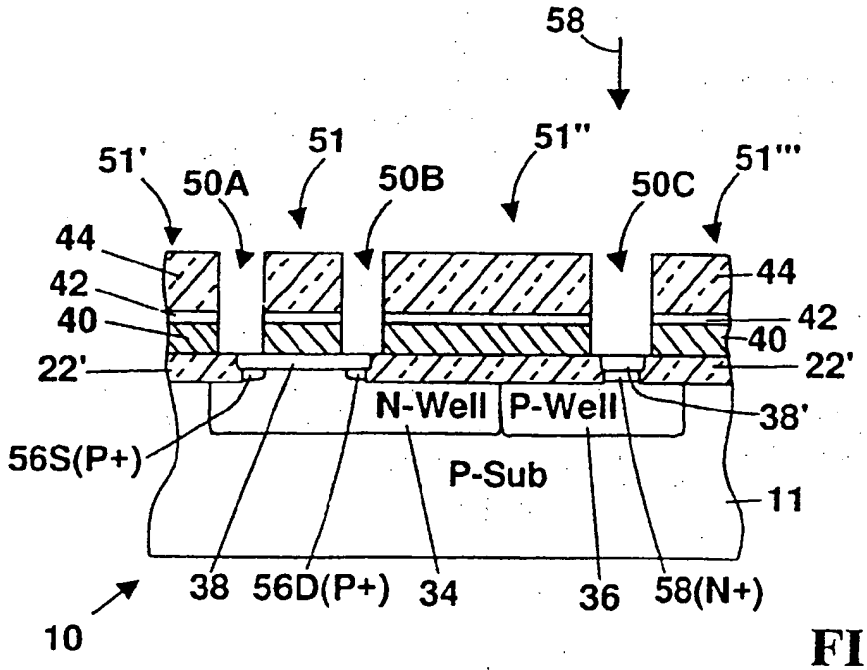



FIG. 1O

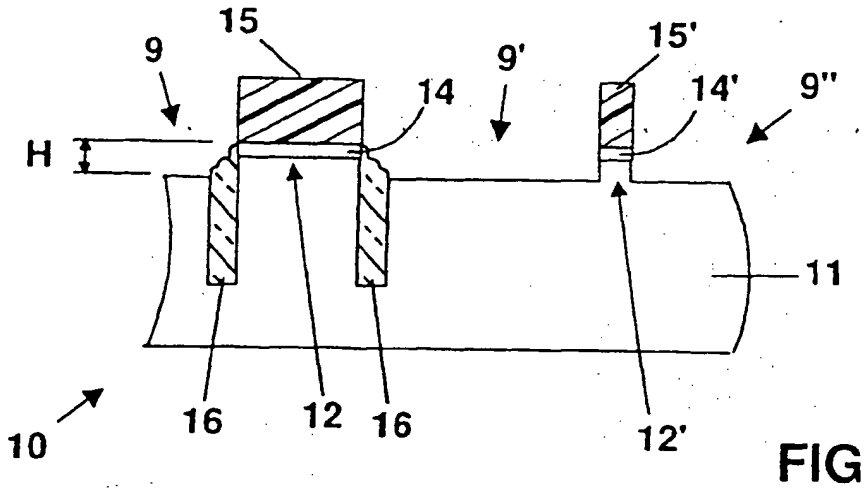



FIG. 2A

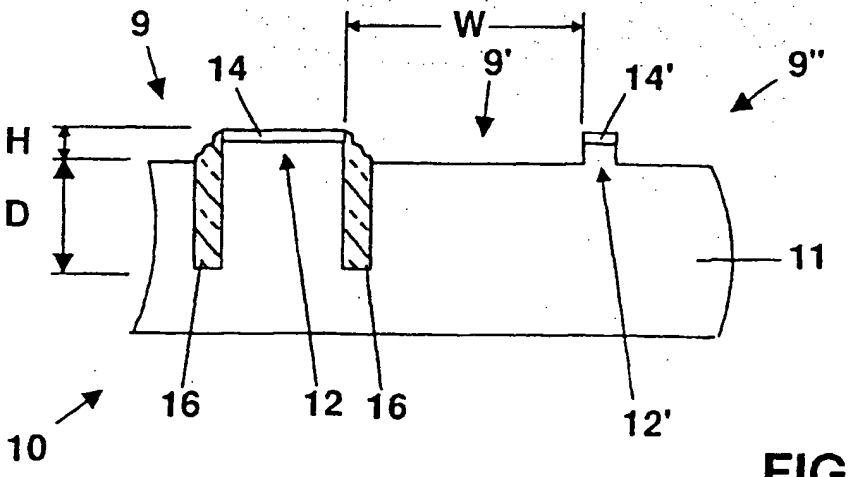



FIG. 2B

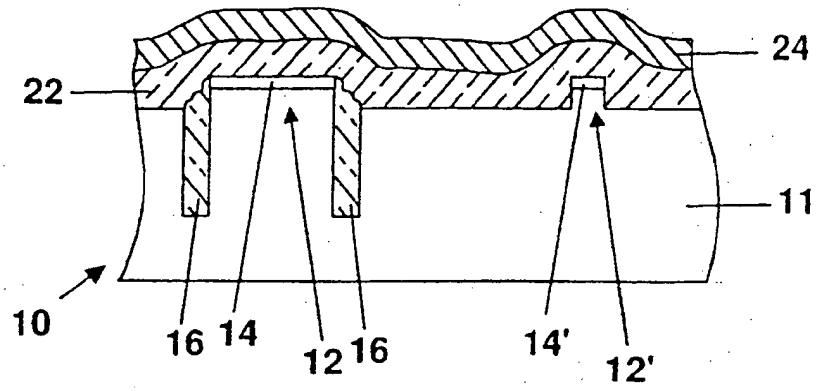



FIG. 2C

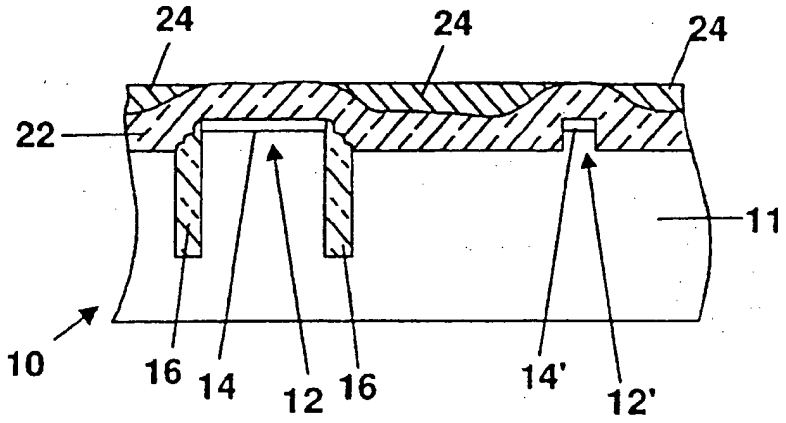



FIG. 2D

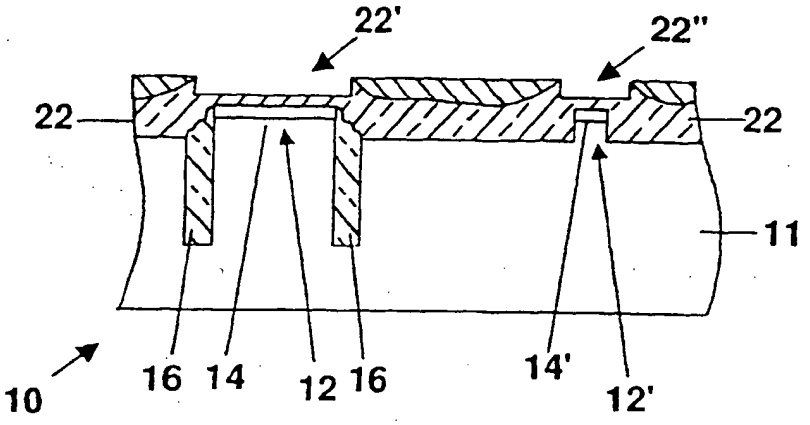



FIG. 2E

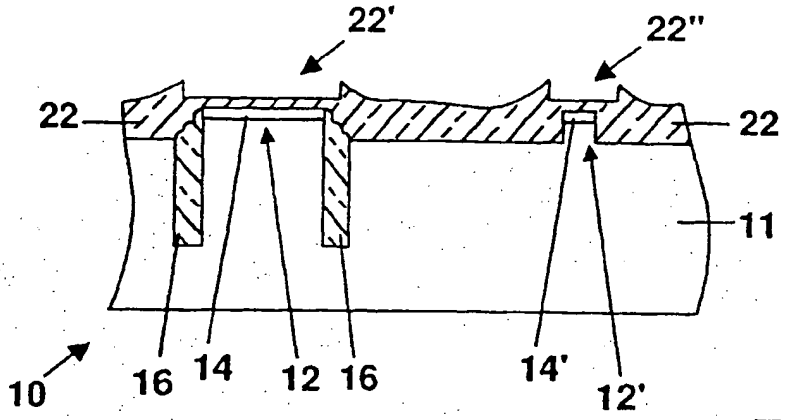



FIG. 2F

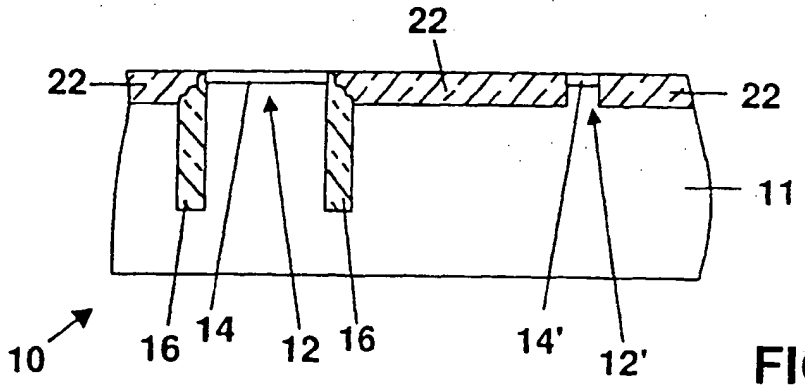
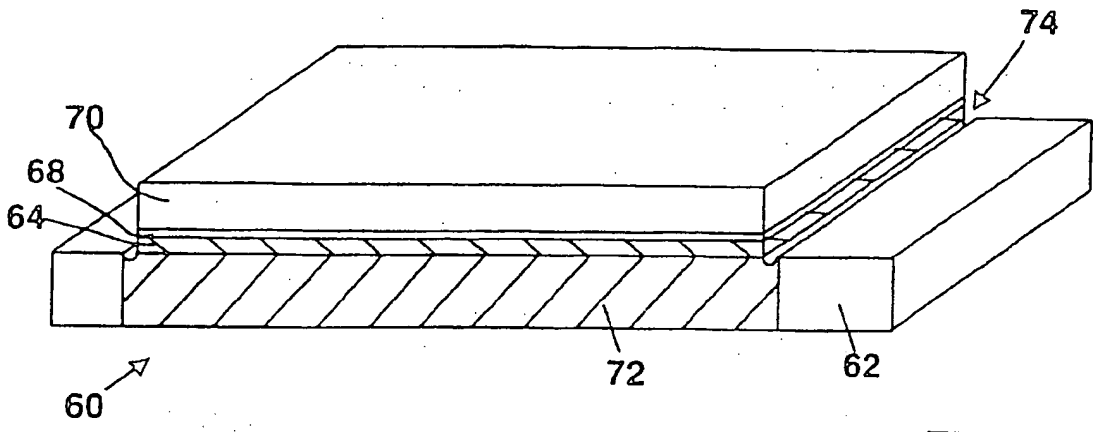



FIG. 2G




PRIOR ART

FIG. 3

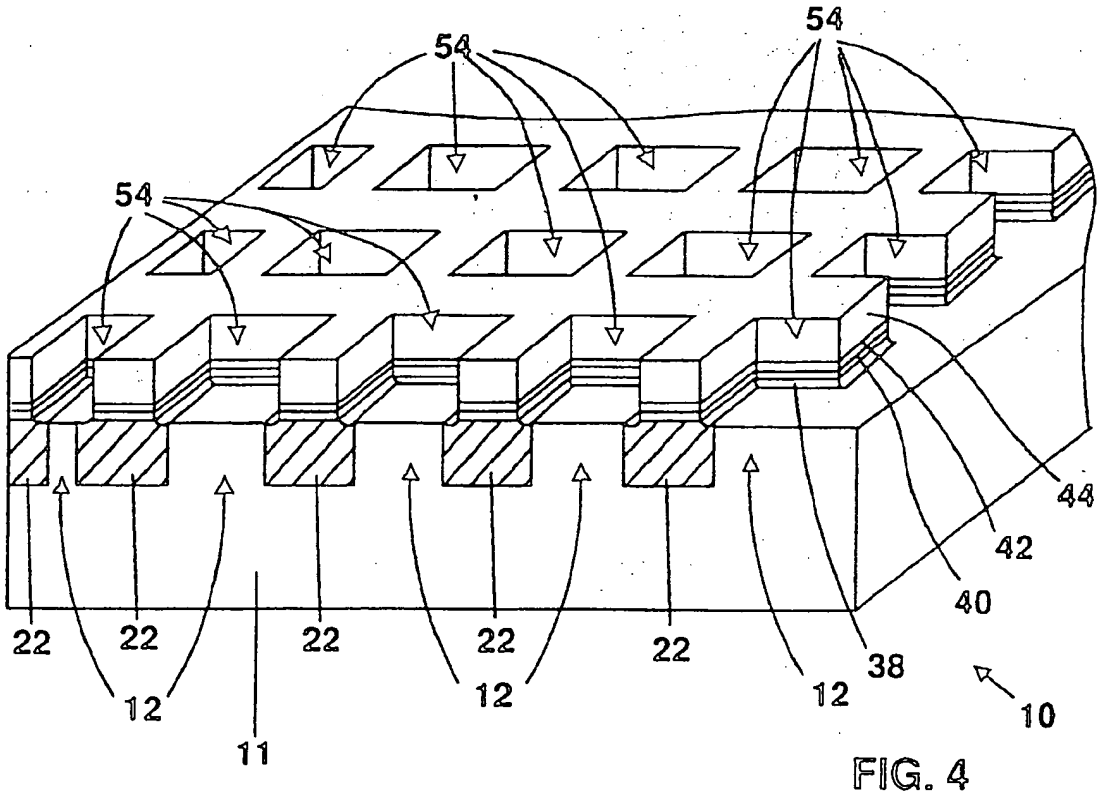



FIG. 4

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European Patent Office
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(11) EP 0 875 927 A3

(12) EUROPEAN PATENT APPLICATION

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**07.07.1999 Bulletin 1999/27**

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**04.11.1998 Bulletin 1998/45**

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# (54) Method of manufacturing FET devices with maskless shallow trench isolation (STI)

(57) FET devices (10) are manufactured using STI on a semiconductor substrate (11) coated with a pad (14) from which are formed raised active silicon device areas and dummy active silicon mesas (12) capped with pad structures on the doped silicon substrate and pad structure. A conformal blanket silicon oxide (22) layer is deposited on the device (10) with conformal projections above the mesas (12). Then a polysilicon film (24) on the blanket silicon oxide layer (22) is deposited with conformal projections above the mesas (12). The polysilicon film projections are removed in a CMP polishing step which continues until the silicon oxide layer (22) is exposed over the pad structures (14). Selective RIE partial etching of the conformal silicon oxide layer (22) over the mesas (12) is next, followed in turn by CMP planarization of the conformal blanket silicon oxide layer (22) which converts the silicon oxide layer into a planar silicon oxide layer, using the pad silicon nitride (14) as an etch stop.

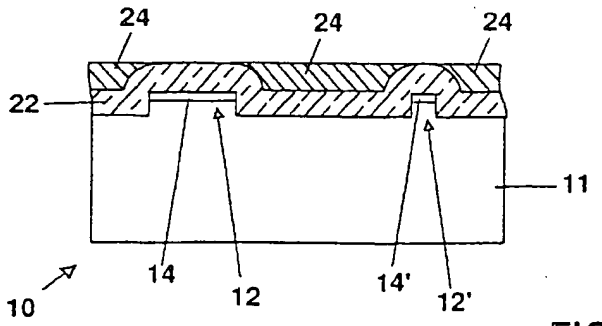


FIG. 1D

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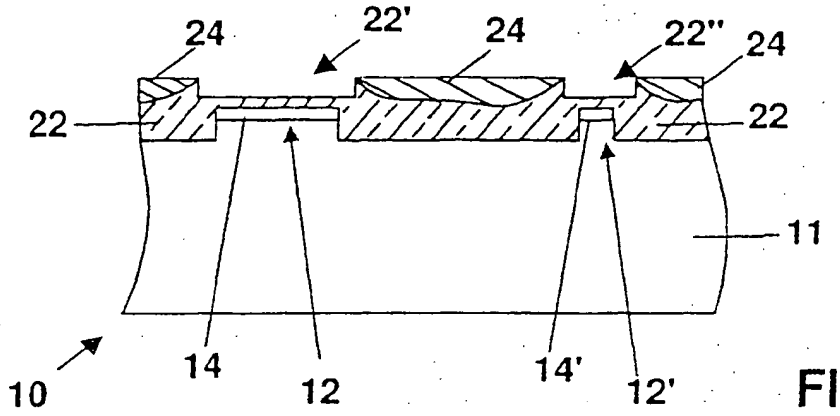


FIG. 1E

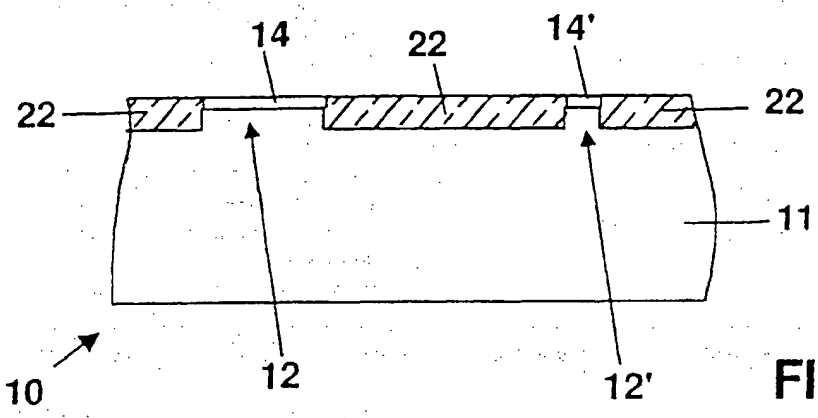


FIG. 1G

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 98 30 3125

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| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
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The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| MUNICH | 4 May 1999 | Werner, A |

CATEGORY OF CITED DOCUMENTS

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L : document cited for other reasons

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04-05-1999

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82